PATENT ABSTRACTS OF JAPAN

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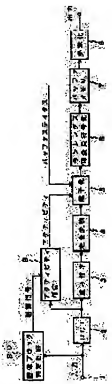
(54) DATA COMPRESSION CIRCUIT

(57)Abstract:

PURPOSE: To improve the picture quality degradation of pictures in which an edge part and a flat part coexist by controlling activity so as to be small by activity control signals and making a qunatization step width small.

CONSTITUTION: DCT coefficients from a DCT(discrete cosine transformation) circuit 2 are supplied to an acitivity judging circuit 9, a maximum AC coefficient within a unit DCT transformation block is calculated and the activity in the DCT transformation block is obtained. Also, input picture information is supplied to a picture block judging circuit 20, a spatial gradient in a picture block is obtained and the activity is controlled corresponding to the size. Since the spatial gradient indicates the sharpness of the edge part, the pictures in which the sharp edge part and the flat part exist can be recognized when the spatial gradient is large. In such time, the activity is controlled so as to be small, the quantization step width becomes narrow, the picture block is finely quantized and the picture quality degration accompanying coarse quantization can be improved.



LEGAL STATUS

[Date of request for examination]

CLAIMS

[Claim(s)]
[Claim 1] The data compression circuit characterized by being made as [control / based on the contents of an image block of an input image / the above-mentioned activity] while facing quantizing a DCT multiplier in a quantization circuit and controlling the quantization step size in the data compression circuit which used DCT conversion based on the magnitude of the activity of an input image at least.
[Claim 2] The data compression circuit according to claim 1 characterized by making activity small in the place where the space inclination of an image block is large, and making it quantization step width of face become narrow.
[Claim 3] The DCT conversion circuit which carries out DCT conversion of the input signal for every unit block in the data compression circuit which used DCT conversion, The 1st weighting circuit which carries out weighting to the above-mentioned DCT multiplier according to a vision property, The quantization circuit which quantizes this DCT multiplier by which weighting was carried out, and the buffer memory which accumulates the quantized DCT multiplier temporarily and is outputted at a fixed rate, The activity judging circuit which computes the activity to the DCT multiplier outputted from the above-mentioned DCT conversion circuit, and is supplied to the above-mentioned quantization circuit by making the value into a quantization step width-of-face control signal, The data compression circuit characterized by consisting of image block judging circuits for input image information being supplied, detecting the space inclination in the unit image block, and controlling the above-mentioned activity.
[Claim 4] The data compression circuit according to claim 3 characterized by using the Laplacian filter as a filter which detects the space inclination in the above-mentioned unit image block.

[Translation done.]

• NOTICES •

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is applied when compressing image data etc. using DCT conversion, and it relates to a suitable data compression circuit, especially the data compression circuit which can improve image quality degradation to an input image with which the edge section and a flat part are intermingled.
[0002]
[Description of the Prior Art] The data compression circuit using the DCT conversion (discrete cosine conversion) technique as a data compression technique of image data is known. Although it quantizes to the DCT multiplier by which DCT conversion was carried out and being changed into the transmission data (compressed data) of a fixed rate in this data compression circuit, quantization step width of face is controlled accommodative, taking into consideration the data occupation of the buffer memory for changing compressed data into a fixed rate at this time, the magnitude of the activity corresponding to the pattern in the unit image block of an input image, etc. (modification).
[0003] Drawing 4 is the schematic diagram showing that conventional example, and DCT conversion within a unit block (usually 8pixelx image block of eight lines) is performed for the input image data supplied to the terminal 1 by the DCT conversion circuit 2 in this data compression circuit 10. In order that the DCT multiplier by which DCT conversion was carried out may carry out weighting according to human being's vision property in the weighting circuit 3, a specific weighting factor is applied. The property that a weighting factor becomes small is given, so that the frequency characteristics of an input image become a high region at this time. The field of a weighting factor is the same magnitude (8x8) as a DCT conversion block.
[0004] As for the DCT multiplier to which the weighting factor according to human being's vision property was given, the DCT multiplier of 2-dimensional ones is changed into the DCT multiplier of a single dimension by the scan conversion circuit 4. Although the single-dimension-ized DCT multiplier is quantized in the quantization circuit 5, the quantization step width of face at this time is controlled accommodative in consideration of [mentioning later] the data occupation of buffer memory 7, or the activity within a DCT conversion block. This is for making it buffer memory 7 not overflow in order to carry out the data compression of the input image in the best condition finally. A DCT multiplier may be single-dimension-ized after quantizing.
[0005] In a run length and the variable-length coding network 6, as for the quantized DCT multiplier, variable-length coding is performed on the basis of a run length. The encoded DCT multiplier (compressed data) is stored in primary by buffer memory 7, and after being made with a fixed rate, it is outputted.
[0006] In the multiplexing circuit 8, status information, an error correction sign, etc. are added to the

encoded DCT multiplier, and it is made with final transmission data, and this transmission data is stored in another memory (illustration is not carried out), or is sent to a data transmission processor (illustration is not carried out) as it is.

[0007] According to the data occupation of buffer memory 7, the quantization step width of face is controlled, and also even if the quantization circuit 5 responds to an activity index, it is controlled. Therefore, the DCT multiplier outputted from the DCT conversion circuit 2 is supplied to the activity judging circuit 9 accompanied by activity index extract processing, and the activity index within a DCT conversion block (DCT resolution picture block) is extracted first.

[0008] Although total of the maximum AC multiplier within a DCT conversion block or AC multiplier etc. is used as an activity index, in this example, the magnitude of activity is judged only with the maximum AC multiplier.

[0009] He is trying for the amount of data by which a quantization curve to which the step size of the quantization circuit 5 becomes large like curvilinear LA–>LB–>LC is chosen and quantized to decrease based on the buffer status information acquired from buffer memory 7 like drawing 5 , so that a data occupation is large. In drawing 5 , a quantization curve can choose it now as a three–stage by buffer status information.

[0010] Quantization step width of face is further controlled according to the magnitude of an activity index. As for activity, activity becomes large, so that a maximum AC multiplier is so large that [that is,] the power of AC multiplier is large. Since human being's vision property also becomes blunt when the power of a DCT multiplier is large, even if it enlarges the step size to quantize, it is seldom influenced by image quality. Therefore, when such, even if it is the same buffer status information, a DCT multiplier is quantized where a quantization step size is enlarged. Drawing 5 shows the example by which a quantization step size is controlled by four steps according to the magnitude of activity.

[0011]

[Problem(s) to be Solved by the Invention] By the way, by the image block with large activity, in controlling on the basis of the magnitude of activity as an activity index, since quantized control which always enlarges a quantization step size is performed, it causes the following problems.

[0012] For example, since the maximum AC multiplier is large, as a result of judging the activity at that time to be a large thing, the quantization step size in this image block will be controlled by image block by which the edge section and a flat part are intermingled by the pattern of a pinstriped pattern as shown in drawing 6 </A> to become large .

[0013] However, in such an image block, if it originally does not quantize finely, image quality degradation will be conspicuous. Especially in an image block from which the brightness of the image of a flat part is changing gently–sloping, since coarse quantization is performed, a false profile will occur, and image quality will deteriorate remarkably.

[0014] So, in this invention, such a conventional technical problem is solved, and when it is the input image with which especially the edge section and a flat part are intermingled, the data compression circuit which can control activity so that fine quantization is performed is proposed.

[0015]

[Means for Solving the Problem] In order to solve an above–mentioned technical problem, while facing quantizing a DCT multiplier in a quantization circuit in the data compression circuit which used DCT conversion and controlling the quantization step size in invention indicated to claim 1 based on the magnitude of the activity of an input image at least, it is characterized by to be made as [control / based on the contents of an image block of an input image / the above–mentioned activity].

[0016] In the data compression circuit which used DCT conversion in invention indicated to claim 3 The 1st weighting circuit which carries out weighting to the above–mentioned DCT multiplier according to a vision property with the DCT conversion circuit which carries out DCT conversion of the input signal for every unit block, The quantization circuit which quantizes this DCT multiplier by which

weighting was carried out, and the buffer memory which accumulates the quantized DCT multiplier temporarily and is outputted at a fixed rate, The activity judging circuit which computes the activity to the DCT multiplier outputted from the above-mentioned DCT conversion circuit, and is supplied to the above-mentioned quantization circuit by making the value into a quantization step width-of-face control signal, It is characterized by consisting of image block judging circuits for input image information being supplied, detecting the space inclination in the unit image block, and controlling the above-mentioned activity.

[0017]

[Function] If invention concerning claim 1 is explained with reference to drawing 1 and drawing 3 , the DCT multiplier outputted from the DCT conversion circuit 2 is supplied to the activity judging circuit 9, in this example, the maximum AC multiplier within a unit DCT conversion block will be computed, and the activity within that DCT conversion block will be called for.

[0018] Input image information is further supplied to the image block judging circuit 20, the space inclination in an image block is searched for, and activity is controlled according to the magnitude. It turns out that it is an image with which the edge section and a flat part sharp when space inclination is large exist since the space inclination in an image block expresses the sharpness of the edge section.

[0019] When such, it is controlled so that activity becomes small. Quantization step width of face becomes narrow by this, and image quality degradation accompanying quantizing finely and quantizing the image block coarsely can be improved.

[0020]

[Example] Then, an example of the data compression circuit concerning this invention is explained to a detail with reference to a drawing about the case where it applies to image data compression. The same sign is given to drawing 4 and a corresponding part, and the detailed explanation is omitted.

[0021] Also in the data compression circuit 10 which starts this invention as an example of this invention is shown in drawing 1 DCT conversion of the picture signal inputted into the terminal 1 is carried out for every unit block by the DCT conversion circuit 2. Through the weighting circuit 3 and the scan conversion circuit 4, the changed DCT multiplier is led to the quantization circuit 5, and is quantized. The configuration by which the quantization step width of face is controlled accommodative based on the activity from the buffer status information and the activity judging circuit 9 of buffer memory 7 is the same as usual.

[0022] In this invention, the space inclination in the image block which the input image information inputted into the DCT conversion circuit 2 is supplied to the image block judging circuit 20, and is going to carry out DCT conversion is computed.

[0023] Since a pattern as shown in drawing 6 is the image with which the edge section and a flat part were intermingled, the space inclination of this image block becomes large, that is, change of that edge section becomes sharp. Activity is controlled by the control signal (activity control signal) which shows the magnitude of the detected space inclination.

[0024] Drawing 2 shows the example of this image block judging circuit 20. The input image information (image data) supplied to the terminal 21 is accumulated in memory 22 for every unit image block. This unit image block is chosen as the same magnitude as the DCT conversion block mentioned above.

[0025] The image data of the image block accumulated in memory 22 is supplied to a filter 23, and the space inclination within the image block is searched for from the image data of an attention pixel and the pixel of the perimeter.

[0026] In order to detect the space inclination of an image block, a differentiation filter is used as a filter 23. In this example, the Laplacian filter which has a multiplication multiplier value as shown in drawing 3 as a differentiation filter 23 is used. This magnitude is arbitrary although the magnitude (the number of taps) of a filter block is (3x3).

[0027] Corresponding to the magnitude of this filter block, from memory 22, an address counter 24 is controlled so that the image data of nine pixels containing an attention pixel is read one by one.
[0028] Since the magnitude of the differential value acquired from a filter 23 expresses the sharpness of space inclination, i.e., the edge section, it is compared with the predetermined threshold Sth to which this differential value is supplied to a comparator circuit 25, and is supplied from a terminal 26.
[0029] In this example, the increment of the counter 27 is carried out with the comparison output obtained when a differential value is smaller than a threshold Sth. That is, it consists of examples so that the number of pixels of the flat part in an image block may be counted. A comparator circuit 25 may be constituted so that the edge section may be counted contrary to this.
[0030] The output of a counter 27 is normalized in the normalization circuit 28. The normalized counter value is as follows.
[0031] normalization counter value = -- the pixel in a counter value (the number of pixels of a flat part) / image block -- since this normalization counter value corresponds to the number of pixels of a flat part, in order to use it as an activity control signal over activity finally a number -- this example -- activity control signal =1.0- (normalization counter value)
•• -- activity is controlled based on the activity control signal changed like.
[0032] In the activity judging circuit 9, the multiplication of this activity control signal is carried out to the maximum AC multiplier computed from the DCT multiplier, and the quantization circuit 9 is controlled by that value as an activity index. For this reason, activity is as follows.
[0033] Activity =(activity control signal) x (maximum AC multiplier)
Therefore, since an activity control signal will take a small value by the image by which the edge section and a flat part are intermingled when there are many flat parts within a unit image block, the activity at this time becomes smaller than the case (conventional example) where the maximum AC multiplier value itself is used. Consequently, since it is controlled so that a quantization step size becomes fine even if it is the same quantization curve, when such an image block inputs, image quality degradation in the part is improvable. For example, even if it is the curve LA shown in drawing 5 , the suitable quantization step size of the inside by the side of LA1 with a quantization step size narrower than the LA4 side is chosen.
[0034] Be [what is necessary / just since the input signal which can be dealt with by this invention is image information and compresses, transmits or accumulates that amount of data], this invention is applicable to all data compression systems.
[0035]
[Effect of the Invention] As mentioned above, in the data compression circuit concerning this invention, activity is computed by taking into consideration not only the activity within a DCT conversion block but the relation between the edge section of an input image block, and a flat part.
[0036] According to this, since it can control so that activity is made small and a quantization step size becomes fine even when it is the image with which the edge section and a flat part are intermingled, it has the description which can improve image quality degradation by such pattern sharply.
[0037] Therefore, this invention is applied when compressing and transmitting the picture signal created with various visual equipments, and it is very suitable.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] This invention is applied when compressing image data etc. using DCT conversion, and it relates to a suitable data compression circuit, especially the data compression circuit which can improve image quality degradation to an input image with which the edge section and a flat part are intermingled.

[Translation done.]

PRIOR ART

[Description of the Prior Art] The data compression circuit using the DCT conversion (discrete cosine conversion) technique as a data compression technique of image data is known. Although it quantizes to the DCT multiplier by which DCT conversion was carried out and being changed into the transmission data (compressed data) of a fixed rate in this data compression circuit, quantization step width of face is controlled accommodative, taking into consideration the data occupation of the buffer memory for changing compressed data into a fixed rate at this time, the magnitude of the activity corresponding to the pattern in the unit image block of an input image, etc. (modification).
[0003] Drawing 4 is the schematic diagram showing that conventional example, and DCT conversion within a unit block (usually 8pixelx image block of eight lines) is performed for the input image data supplied to the terminal 1 by the DCT conversion circuit 2 in this data compression circuit 10. In order that the DCT multiplier by which DCT conversion was carried out may carry out weighting according to human being's vision property in the weighting circuit 3, a specific weighting factor is applied. The property that a weighting factor becomes small is given, so that the frequency characteristics of an input image become a high region at this time. The field of a weighting factor is the same magnitude (8x8) as a DCT conversion block.
[0004] As for the DCT multiplier to which the weighting factor according to human being's vision property was given, the DCT multiplier of 2-dimensional ones is changed into the DCT multiplier of a single dimension by the scan conversion circuit 4. Although the single-dimension-ized DCT multiplier is quantized in the quantization circuit 5, the quantization step width of face at this time is controlled accommodative in consideration of [mentioning later] the data occupation of buffer memory 7, or the activity within a DCT conversion block. This is for making it buffer memory 7 not overflow in order to carry out the data compression of the input image in the best condition finally. A DCT multiplier may be single-dimension-ized after quantizing.
[0005] In a run length and the variable-length coding network 6, as for the quantized DCT multiplier, variable-length coding is performed on the basis of a run length. The encoded DCT multiplier (compressed data) is stored in primary by buffer memory 7, and after being made with a fixed rate, it is outputted.
[0006] In the multiplexing circuit 8, status information, an error correction sign, etc. are added to the encoded DCT multiplier, and it is made with final transmission data, and this transmission data is stored in another memory (illustration is not carried out), or is sent to a data transmission processor (illustration is not carried out) as it is.
[0007] According to the data occupation of buffer memory 7, the quantization step width of face is controlled, and also even if the quantization circuit 5 responds to an activity index, it is controlled. Therefore, the DCT multiplier outputted from the DCT conversion circuit 2 is supplied to the activity judging circuit 9 accompanied by activity index extract processing, and the activity index within a DCT

conversion block (DCT resolution picture block) is extracted first.

[0008] Although total of the maximum AC multiplier within a DCT conversion block or AC multiplier etc. is used as an activity index, in this example, the magnitude of activity is judged only with the maximum AC multiplier.

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[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, in the data compression circuit concerning this invention, activity is computed by taking into consideration not only the activity within a DCT conversion block but the relation between the edge section of an input image block, and a flat part.
[0036] According to this, since it can control so that activity is made small and a quantization step size becomes fine even when it is the image with which the edge section and a flat part are intermingled, it has the description which can improve image quality degradation by such pattern sharply.
[0037] Therefore, this invention is applied when compressing and transmitting the picture signal created with various visual equipments, and it is very suitable.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the schematic diagram showing an example of the data compression circuit concerning this invention.
[Drawing 2] It is the schematic diagram showing the example of an image block judging circuit.
[Drawing 3] It is drawing showing an example of a differentiation filter.
[Drawing 4] It is the schematic diagram of the conventional data compression circuit.
[Drawing 5] It is the property Fig. showing the example of control of a quantization step size.
[Drawing 6] It is drawing showing the example of an image for which the edge section and a flat part are intermingled.
[Description of Notations]
2 DCT Conversion Circuit
3 Weighting Circuit
4 Scan Conversion Circuit
5 Quantization Circuit
6 Run Length and Variable-length Coding Network
7 Buffer Memory
8 Multiplexing Circuit
9 Activity Judging Circuit
10 Data Compression Circuit
20 Image Block Judging Circuit

[Translation done.]